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(54) Information processing system.

(57) A method and apparatus for powering down a computer system while saving the state of the system at power down is disclosed. The system maintains the capability to suspend the execution of an application program operating on the system at any point and resuming execution of the application program at that same point at a later time. The time at which the system may be powered down and then powered back up again is totally arbitrary and depends only upon the user of the system. At the time the system is powered off, the contents of all active registers as well as the states of all I/O devices in the system are stored in a special save area of system memory. This special save area is provided with power during the suspended time in order to retain the state of the system at the time it was powered down. By using this special save suspend area, the main memory area of the system is available to any application programs independently of the system save memory requirements. Additionally, the system may be powered on and off under software control thereby providing the capability for unattended system operation using an alarm function.

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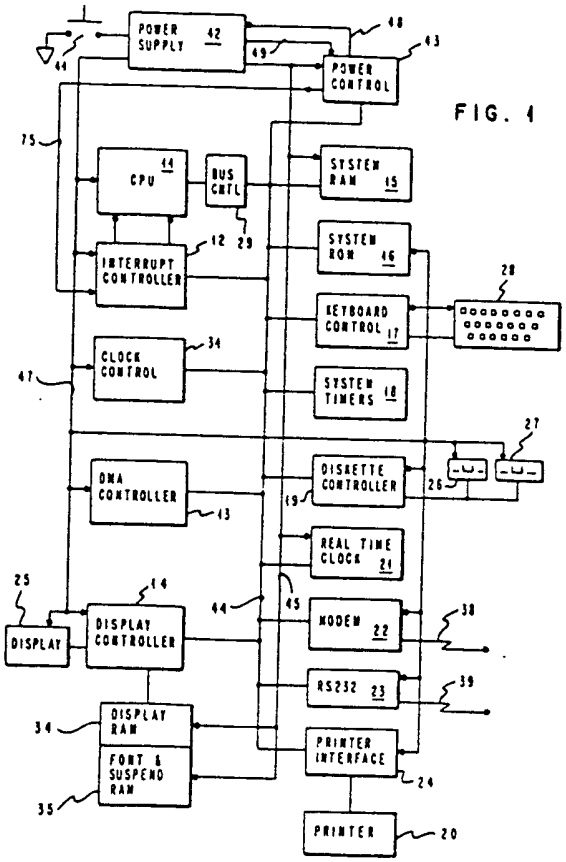
POWER SUPPLY 42
48
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POWER CONTROL
44
75
CPU 44
BUS CNTL
SYSTEM RAM 15
INTERRUPT CONTROLLER
12
29
SYSTEM ROM 16
28
KEYBOARD CONTROL 17
CLOCK CONTROL
34
47
SYSTEM TIMERS 18
27
DMA CONTROLLER
13
DISKETTE CONTROLLER
19
26
REAL TIME CLOCK 21
25
14
44
45
DISPLAY
DISPLAY CONTROLLER
MODEM 22
38
RS232 23
39
34
DISPLAY RAM
FONT & SUSPEND RAM
35
PRINTER INTERFACE
24
PRINTER
20

FIG. 1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 87 30 0121

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
A,D	US-A-4 458 307 (J.C. McANLIS) * Column 1, line 55 - column 2, line 19 *	1	G 06 F 1/00
A	US-A-4 327 410 (R.S. PATEL) * Column 1, line 49 - column 2, line 4; claim 1 *	1,3	
A	PATENT ABSTRACTS OF JAPAN, vol. 9, no. 37 (P-335)[1760], 16th February 1985; & JP-A-59 178 694 (HITACHI SEISAKUSHO K.K.) 09-10-1984	1,3	
A	PATENT ABSTRACTS OF JAPAN, vol. 8. no. 208 (P-302)[1645], 21st September 1984; & JP-A-59 90 295 (NIPPON DENKI K.K.) 24-05-1984	1,3,7,8	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

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G 06 F 11/14

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23-06-1989	ALONSO Y GOICOLEA L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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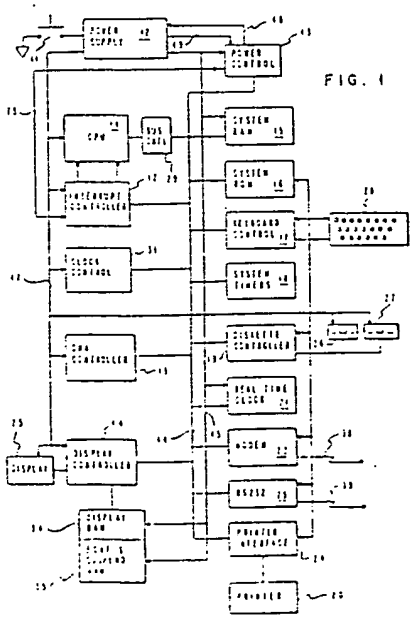

FIG. 1

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Description

INFORMATION PROCESSING SYSTEM

This invention relates to the powering on and off of a computer system, and more particularly to the capability to suspend and resume a software application running on the computer system during a power off/on cycle.

In the information processing environment, it would be very valuable to be able to suspend and resume programs running on a central processing unit (CPU) during times when the CPU is powered off and on. It would be especially valuable to be able to resume the programs at the exact execution point at which they were suspended during a power off occurrence. The ability to suspend and resume an application program during a power off/power on cycle is very important for a portable computer. A typical user of such a portable computer would most likely be cycling his computer off and on much more frequently than a user of a computer that is fixed in one location. It would be very desirable and highly productive for the user of such a portable computer to be able to instantly power on and resume system operation at the point at which execution was suspended.

A further advantage of such a suspend and resume feature is found in the battery operated computer field. By eliminating the restarting of a program from the beginning, battery life would be extended by eliminating the disk drive operations usually required for an application and a data base which have to be reloaded at power on.

A major requirement for such a suspend and resume feature is that the state of the CPU and the computer registers and peripherals must be interrogated and stored at the suspend time so that they may be re-stored accurately at the time of resumption. Consequently in effect the entire system's state must be saved including control and memory mechanisms associated with the display, system timing mechanisms, interrupt and keyboard controllers, as well as communication controllers. A second major requirement to be able to perform an accurate suspend/resume function is that the contents of the memory must be retained. As part of this latter requirement, some power must be supplied to the memory while the system is off in order to save its contents. As part of this saving requirement, it would be desirable for the system's state to be saved in a special area separate from main memory that is not accessible to any application programs running on the system. In this manner, main memory space is not used up during a suspend/resume operation.

Large computing systems have been known to have some type of early-power-off warning system to enable the computing system to go down without destroying large quantities of data. However, none of these systems has the capability to restore the hardware to its pre-power down state. Typically, what is done is that the system is restarted and reloaded from the beginning. U. S. Patent 4,458,307 discloses a data processing system having a volatile main memory which includes a data save controller for protection against loss of the memory during a power failure. At the first sign of a power supply failure, non-postponable tasks are completed and data saving is accomplished by storing the contents of volatile processor registers in the main memory area. At the conclusion of a power failure, the contents of the main memory are then transferred back to the volatile registers for reinitialization and restart. Power fault detection circuitry is required to detect a power failure sufficiently in advance to be able to transfer from volatile to non-volatile storage areas.

A similar technique is found in U. S. Patent 3,959,778 wherein data is transferred from a volatile main memory of a data processor to a peripheral permanent storage unit upon failure of the main supply to the data processor. Circuitry is provided to read the contents of the main memory into the selected permanent storage unit within a time period short enough so that perishable data in the main memory is not lost.

U. S. Patent 4,096,560 describes a protection circuit which disables control signals to a microprocessor and to a memory to prevent the loss of stored data from the memory during power fluctuations. The control signals inhibit the reading or writing of data into the memory and maintain the microprocessor in a reset mode of operation during the power level fluctuations and interruptions.

In accordance with the invention, an apparatus and method are provided for enabling a user of a computer system to suspend execution of a program by powering down the system while maintaining the capability to restart execution at the exact point at which it was suspended after powering back on. The user of such a system may arbitrarily suspend execution at any point in time and similarly resume execution at any point in time without having to restart and reload the program that was running on the system at the time it was powered down. At the time the computer system is powered down, the contents of all active registers as well as the states of all I/O devices in the system are stored in a special save area of the memory. This special save area is provided with power during and after the suspend operation, thereby retaining the state of the machine while it is powered down.

The computer system disclosed herein includes a display, memory, timers, interrupt apparatus, a keyboard, and communication devices. Consequently, at the time the system is powered down, the entire state of the machine must be saved including that of the display controller, the memory, system timers, interrupt controllers, keyboard controllers, communication controllers and central processor registers. The computer system state is saved in a special save area that is not accessible to any application program running on the system. As a result of this, all of the main memory area is available to application programs independently of the system save requirements demanded by the special system

save area.

As an additional capability, the computer system may be powered on and off under software control. Attendant with the capability to power on and off under software control is the capability to allow unattended operation of the computer system. A time of day alarm function built into the system enables the system to be powered on, and resumed at predetermined times.

In order that the invention may be fully understood a preferred embodiment thereof will now be described with reference to the accompanying drawings in which:

Fig. 1 is a functional block diagram of the system according to the present invention.

Fig. 2 is a block diagram of the power control section used to power down and power up the system according to the present invention.

Figs. 3a-3c are flow charts depicting the operations which occur during a power down operation.

Figs. 4a-4e are flow charts depicting the powering back on of the system following a power off sequence.

Referring now more particularly to the drawings, the overall system of the invention is shown in Fig. 1. Continuous power is supplied from power supply 42 to power control 43 over line 45. As can be seen, continuous power is also supplied from power supply 42 on line 45 to system RAM 15, real time clock 21, display RAM 34 and display font/suspend RAM 35. The operation of on/off switch 41 to power supply 42 controls the operation of line 49 which communicates between power supply 42 and power control 43. When on/off switch 41 is depressed, line 49 causes power control 43 to provide a power enable signal over line 48 to power supply 42. In this manner, switched power is provided over line 47 to CPU 11, interrupt controller 12, clock control 31, DMA controller 13, display controller 14 and display 25. Power control 43 also provides a suspend non-maskable interrupt (NMI) to interrupt controller 12. Note that switched power is also provided on line 47 to system ROM 16, keyboard control 17 and keyboard 28, diskette controller 19, diskette drives 26 and 27, modem 22, RS232 communication interface 23 and printer interface 24.

Modem 22 communicates with an external device over line 38 and the RS232 interface 23 communicates with an external device over line 39. Bus controller 29 controls the flow of data among the following devices: power control 43, CPU 11, interrupt controller 12, clock control 31, DMA controller 13, display controller 14, printer interface 24, RS232 communication interface 23, modem 22, real time clock 21, diskette controller 19, system timers 18, keyboard control 17, system ROM 16 and system RAM 15. As can be seen, the communication of data among these aforementioned devices transpires over bus 44. Note also there is data communication between display controller 14 and display 25, between diskette controller 19 and diskette drives 26 and 27, and between keyboard control 17 and keyboard 28.

The suspend and resume operations during a power on/off cycle will now be described in more detail with respect to Figs. 3a-3c and 4a-4e, respectively. In operation, when power on/off switch 41 is depressed, a suspend NMI is generated to initiate the saving of the system's present state within approximately a two second time period. As shown in step 84, the first operation performed subsequent to power switch 41 being depressed is to save the contents of all of the registers of CPU 11. Subsequently, all system interrupts are disabled and a system suspend flag is cleared as depicted in step 85. The clearing of the system suspend flag prevents the system from being restarted from the beginning when the system is resumed unless the system is successfully suspended. As indicated in step 86, the diskette drives and the display are turned off and any printer operation is stopped while any audio output is disabled.

In step 87, a system profile area in RAM 15 is read. In this area, a user of the system can indicate that it is desired to have the system restart from the beginning of any suspended application program rather than having it resume at its suspended execution point. In decision block 88, a determination is made as to whether or not a resume mode is set, i.e., whether or not the system will resume at the suspended execution point. If the answer is no, then a second determination is made as to whether or not a "force" resume is set. This is done in block 89. A "force" resume overrides the information in the system profile area that was read in step 87 so as to force the system to resume at its suspended execution point. This "force" resume would be used to prevent loss of the system's state if the power supplied to the system were in danger of running out. In the preferred embodiment disclosed herein, the power is supplied to the system by a battery, i.e., power supply 42 is a battery. In this manner, the state of the system can be saved if the battery runs low during the execution of an application program without losing data which cannot be recovered. If the answer to decision block 89 is no, then no saving of the system is done in the event of power off. However, if the answer to either decision block 88 or decision block 89 is yes, then as indicated in step 91, a special save area in RAM 35 is activated. In accordance with the activation of this special suspend save area in RAM 35, the real time clock 21 interrupt mode is saved and all real time clock interrupts except an alarm interrupt are disabled, i.e., only the alarm function of the system has power remaining on. In decision block 93, a determination is made as to whether or not an alarm power-on-activation has been requested. If there are no alarms set, then operation proceeds to step 95 which will be explained with respect to Fig. 3b. However, if an alarm power-on has been requested, then as indicated in step 94, the alarm hardware provides an enable-power-on so that at the time an alarm goes off, if the system has been suspended it will then resume execution at the point at which it was suspended.

Having made a determination as to whether or not a resume mode has been set and a second determination as to whether or not an alarm function

is required, a number of functions are carried out subsequent to step 95. These are as shown in Fig. 3b. As indicated in step 96, the stack segment and stack pointer registers within CPU 11 are saved. As indicated in steps 97 and 98, the state of the display controller 14 and the state of system timers 18 is each saved. As shown in steps 101 and 102, the registers of both interrupt controller 12 and DMA controller 13 are saved. Additionally, (as shown in step 103) all interrupt vectors which are used by the system to perform a power on self test (POST) when the system is restarted are saved. To facilitate the POST, the main area in RAM 15 used by POST is saved as disclosed in step 104. Finally, as shown in step 105, the state of the registers of keyboard control 17 is saved.

The saving of the system's state continues as shown in step 106 in Fig. 3c. Each of modem 22 and RS232 communication interface contains controller setup registers for holding information which is desired to be communicated over lines 38 and 39, respectively. Modem 22 is considered the primary communication device while RS232 communication inter- face 23 is considered the secondary communication device. As shown in steps 107 and 108, the registers containing information which is to be communicated is saved at the time of power down or system suspend. Note that any information that is being communicated over lines 38 and 39 at the time of a power down will be lost. Additionally, as shown in steps 109 and 110, both the main memory and the special suspend memory have a check sum procedure performed on them and their contents are stored in the special save area. These operations are done to make sure that the contents of memory have not changed during the suspend operation. Finally, in steps 111 and 112, a system suspend flag is set, further execution is halted and the system waits for the expiration of the two second time period after the suspend operation has been initiated. Further operation then halts until a system resume operation is initiated.

Figs. 4a-4e depict the operations and functions performed during a power on resume operation. Once again, it is to be noted that a successful power on resume operation enables the application program that was running on the computer system to begin executing at the exact point at which execution ceased at the time the power down suspend operation was performed. As indicated in step 113, power is restored to the system either by an operator pressing on/off switch 41 or by a preset alarm. In step 114, a hardware reset flag is read in order to determine whether or not the user wishes to run a new application program, thereby aborting the resumption of the system's state at power down. If no reset flag has been set, then the resumption process will proceed at the last execution point. In decision block 115, a determination is made as to whether or not there has been either an operator or battery loss abort, thereby indicating the reloading of the application program at its beginning. If either of these conditions occur, then a system suspend flag is reset as shown in step 116. However, if neither of these conditions occur, then the suspend save area in RAM 35 is accessed and a checksum function is performed. If the checksum function indicates an error, then the system suspend flag is reset and the application restarts at the beginning and not at the previous execution point. However, if the checksum of the suspend save area is successful, then a checksum function is performed on the main memory of RAM 15 as indicated in step 121. Once again, if there is an error found, then the system suspend flag is reset, an error code is issued, and the application program must restart at the beginning. However, if the latter checksum operation is successful, then a determination is made in decision block 125 (see Fig. 4b) as to whether or not a suspend flag has been set. If a suspend flag has not been set, then the state of the system must be re-stored to its beginning.

As indicated in step 126, a complete POST function is performed and all memory is cleared. Subsequently, any errors which have occurred are displayed as shown in step 128 and a determination is made as to whether or not any fatal errors have been found. If any fatal errors have been found, then the system is shut down. However, if no fatal errors have been found, then an initial program load is done on the system from one of diskette drives 26 or 27 and control is then passed to the particular application program which has been loaded into the system.

The yes branch of step 125 follows if the application program that was suspended is to be resumed at its previous execution point. In step 127, a power on self test (POST) is performed without significantly modifying the main memory of RAM 15 and without modifying font/suspend RAM 35 and display RAM 34. However, if any fatal errors have been found as shown in decision block 33, then the errors are displayed and the system is shut down. When no fatal errors have been found, then resumption proceeds with all interrupts being disabled and the suspend save area in RAM 35 being accessed. Additionally, the registers of display controller 14, and system timers 18, are restored to their previous states as shown in steps 135 through 137. The resumption process continues with step 139 as shown in Fig. 4c. At this point, interrupt controller 12 is re-stored and the main memory area of RAM 15 which was used by POST is also restored. Additionally, any key depressed flags of keyboard 20 are cleared and any pending keys in keyboard 28 are purged, while the system configuration information is updated due to possible changes while powered off. Finally, the registers of keyboard control 17 are restored.

Continuing, the communication setups of modem 22 and RS232 communication interface 23 are restored as shown in steps 147 and 148 (see Fig. 4d). Next, the stack segment and stack pointer registers of CPU 11 are restored and the suspend save area in RAM 35 is disabled so that at this point application program access to this space is prohibited.

In decision block 152, a determination is made as to whether or not the system has been powered back on by an alarm that has been previously set. If the answer is affirmative, then the alarm of real time

clock 21 is reset and a memory flag set, thereby informing the application program that is currently loaded that the system is currently unattended by a user. Continuing, the printer 20 is enabled. Finally, in step 155, the capability of the system to once again suspend an application program is enabled.

The last operations which are performed to complete the resume operation are detailed in Fig. 4e. In step 157, a change flag on both diskettes 26 and 27 is set to force the operating system program to check that the correct diskette is loaded in one of diskette drives 26 or 27 before a write operation proceeds. This is to assure that the diskette that will be written on is the same one that was being written on at the time the suspend operation was initiated. The state of diskette controller 19 could be saved and restored, however, in the best mode of this invention, it is not because the operation will be aborted with "possible diskette changed" status and it is up to the operating system to validate the diskette and retry the operation. Subsequently, a resume call is issued to the operating system program thereby allowing restoration of printer 20 to its previous state and enabling an updating of the present time and date from real time clock 21. By so doing, the correct time and date may be shown on display 25. All registers in CPU 11 are restored from the stack and a signal is provided to display controller 14 to enable video data to be shown on display 25. Finally, a return from the suspend interrupt is executed and the application program that was suspended is resumed at its previous execution point.

The operation of the logic used to control the powering down of the system during a system suspend operation will be explained in more detail hereinafter with respect to Fig. 2. When the power control circuit of Fig. 2 is first powered on, flip-flops 62, 65, 66 and 69 are all reset using the system reset signal on line 73. The power enable signal on line 48 is at a low logic state thereby indicating that the rest of the system is not powered on. In order to activate the power enable signal on line 48 to turn on the system, power switch 41 is depressed which in turn places a pulse on the power switch signal of line 49. Alternatively, the system may be turned on by a real time clock alarm signal on line 72 going to a low logic state thereby signaling the turning on of power by the alarm function. Flip-flop 62, which is a toggle-type flip-flop, will then change states causing the signal on line 70 to go from a high logic state to a low logic state. Since the set input for flip-flop 65 is on line 70, flip-flop 65 is then set and the power enable signal on line 48 becomes active.

When the system is powered on, a reset signal is generated by the circuit of Fig. 2 in the following manner. When the signal on line 70 transits from a high to a low logic state, a 250 millisecond count is begun. After 100 milliseconds have elapsed, the signal on line 82 is raised to a high logic state thereby causing flip-flop 66 to clock in a high signal for the reset signal of flip-flop 66. After the 250 millisecond time period has elapsed, the signal on line 83 goes to a low state which resets flip-flop 66 thereby causing the reset signal of flip-flop 66 to go to a low state. Consequently, 100 milliseconds after the power enable signal becomes active, the reset signal will become active for a period of 150 milliseconds.

To turn off the computer system, power switch 41 is again depressed, and another pulse is placed on the power switch signal on line 49. Note that the system may also be powered off by a software request, thereby causing the software power-off signal on line 74 to go to a low state thereby providing a reset signal to flip-flop 62. Flip-flop 62 then changes state thereby causing the signal on line 70 to transit from a low to a high state. As a result, flip-flop 65 which has the signal on line 70 as its set input, is not then being set and can therefore be clocked. Divide down counter 61 then counts up to 2 seconds and it raises its 2 second output signal on line 81 which clocks in a low signal to flip-flop 65. This low signal disables power.

During a powering-off sequence, a system suspend NMI signal on line 75 is generated to signal any software running on the system that a power down sequence is now underway. This signaling process is accomplished using pulse generator 64. When the signal on line 70 transits from a low to a high state, pulse generator 64 generates a pulse which sets flip-flop 69 thereby causing line 75 to go to a high state thereby signaling the software to begin the suspend sequence.

Claims

1. An information processing system including a central processor, memory, and a plurality of input-output devices, characterised in that the system further includes

means for powering-off said information processing system;

means for saving the state of all memory locations and of each of said plurality of input-output devices when said powering-off means are activated; and,

means for restoring all memory locations and each of said plurality of input-output devices to the state held at power-off time upon powering said information processing system back on.

2. An information processing system according to claim 1 wherein said means for powering-off said information processing system comprises means for disabling all interrupts in said system and for halting operation of each of said plurality of input-output devices.

3. An information processing system according to claim 1 or claim 2 wherein said saving means comprises means for activating an isolated area of memory for storing the state of selected memory locations and of each of said plurality of input-output devices.

4. An information processing system according to claim 3 further including means for performing a checksum operation on said special area of memory as well as on the remainder of said memory.

5. An information processing system according to claims 2, 3 or 4 further comprising means for setting a system suspend flag subsequent to the disablement of all system interrupts and the turning off of each of said plurality of input-output devices.

6. An information processing system according to any of the preceding claim 1 further comprising means for disabling said saving means and said restoring means upon powering-off said information processing system.

7. An information processing system including, a central processor on which an application program executes, memory and a plurality of input-output devices, said information processing system characterised in that the system comprises

means for powering-off said information processing system and suspending execution of an application program;

means for saving the state of all memory locations and of each of said plurality of input-output devices at said power-off time;

means for restoring all memory locations and each of said plurality of input-output devices to the state held at said power-off time upon powering said information processing system back on; and,

means for resuming execution of said application program at the point at which it was suspended.

8. An information processing system according to Claim 7 wherein said saving means comprises means for activating a special memory area for storing the state of selected memory locations and of each of said plurality of input-output devices.

9. An information processing system according to claim 8 further comprising means for performing a checksum operation on said special area and on the remainder of said memory.

10. An information processing system according to claim 9 further comprising means for disabling said restoring means upon the occurrence of an error during said checksum operation.

11. A method for suspending and resuming operation of an information processing system characterised by

powering-off said information processing system;

saving the state of all memory locations and each of said plurality of input-output devices at power-off time; and,

restoring all memory locations and each of said plurality of input-output devices to the state held at power-off time upon powering said information processing system back on.

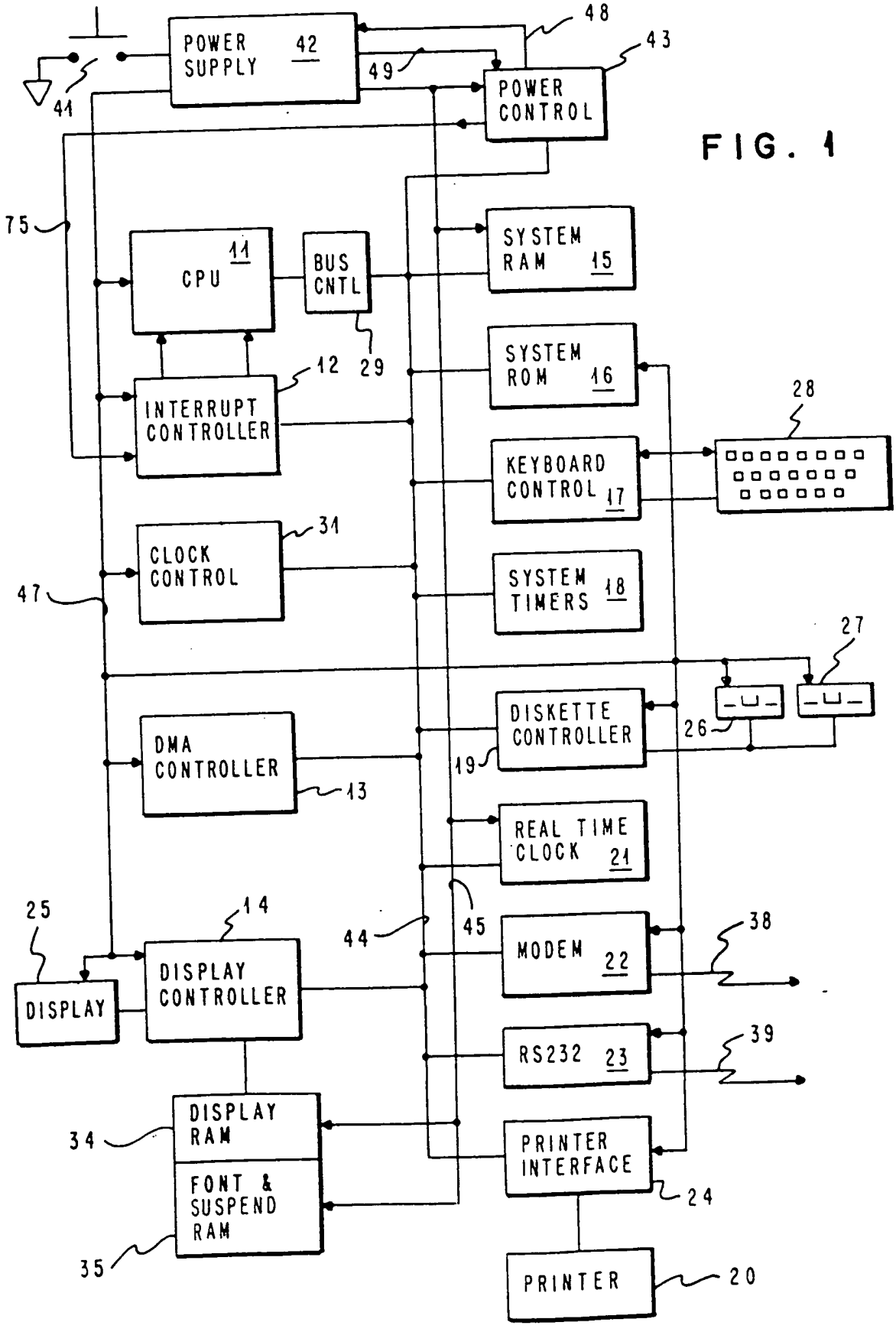
12. A method for suspending and resuming an application program executing on an information processing system characterised by:

powering-off said information processing system thereby suspending execution of an application program;

saving the state of all memory locations and of each of said plurality of input-output devices at said power-off time;

restoring all memory locations and each of said plurality of input-output devices to the state held at said arbitrary time upon powering said information processing system back on; and,

resuming execution of said application program at the point at which it was suspended.


POWER SUPPLY 42
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SYSTEM ROM 16
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KEYBOARD CONTROL 17
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CLOCK CONTROL
47
SYSTEM TIMERS 18
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DISKETTE CONTROLLER
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DMA CONTROLLER
13
REAL TIME CLOCK 21
25
14
44
45
MODEM 22
38
DISPLAY
DISPLAY CONTROLLER
RS232 23
39
DISPLAY RAM
34
PRINTER INTERFACE
24
FONT & SUSPEND RAM
35
PRINTER
20

FIG. 1

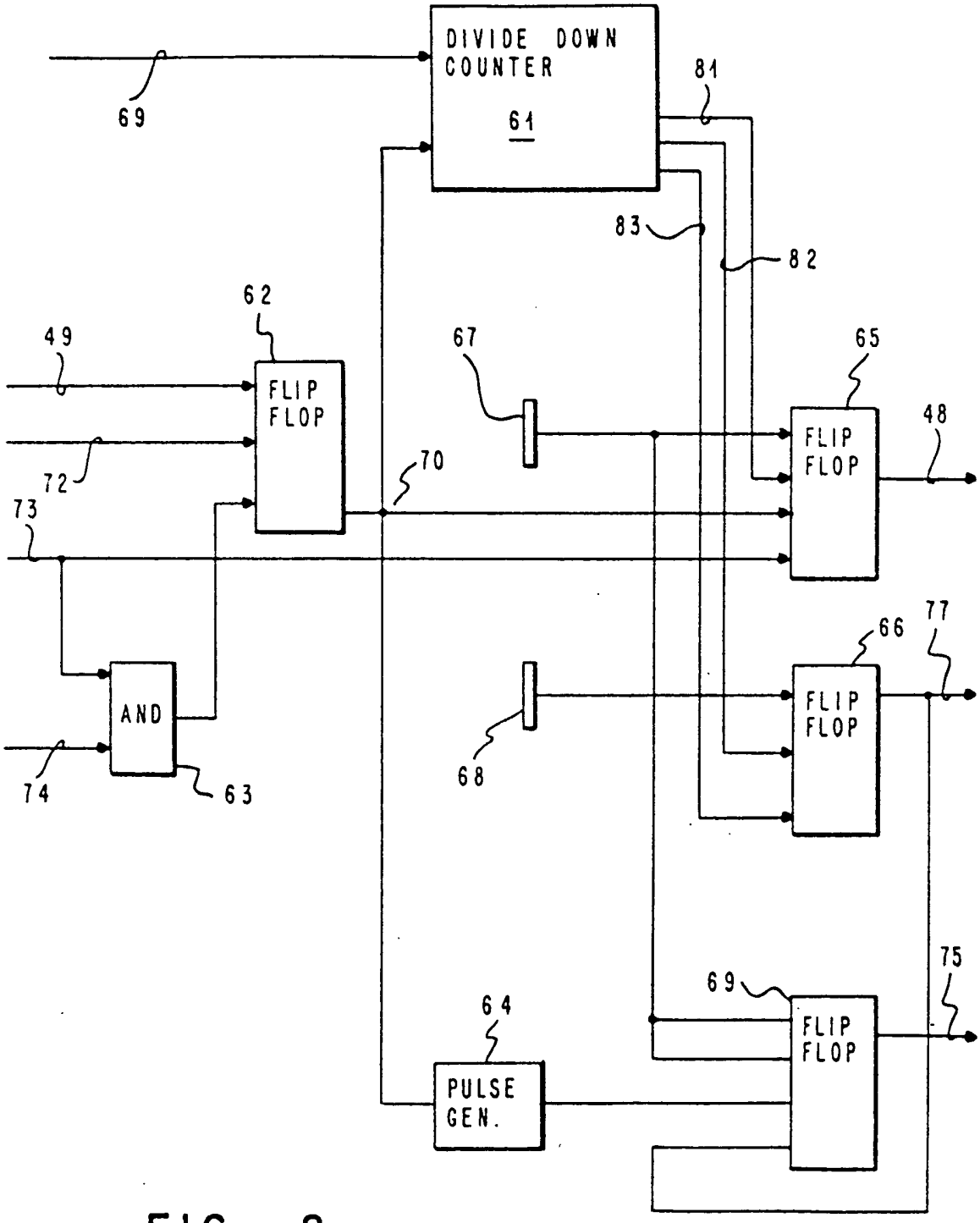
DIVIDE DOWN COUNTER
61
69
81
83
82
62
49
FLIP FLOP
67
65
48
72
70
73
FLIP FLOP
66
77
AND
74
63
68
FLIP FLOP
75
69
64
PULSE GEN.
FLIP FLOP

FIG. 2

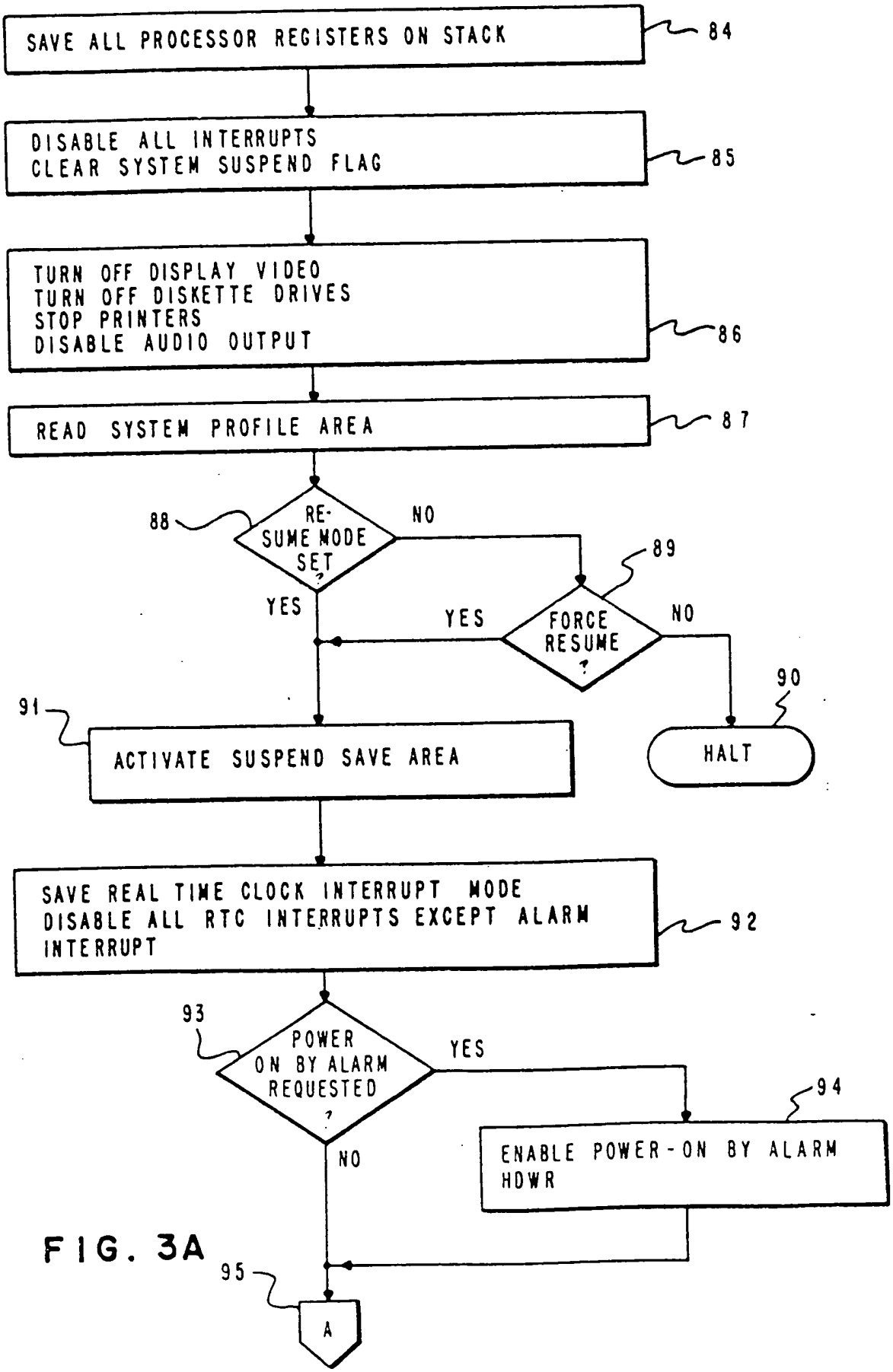
SAVE ALL PROCESSOR REGISTERS ON STACK
84
DISABLE ALL INTERRUPTS
CLEAR SYSTEM SUSPEND FLAG
85
TURN OFF DISPLAY VIDEO
TURN OFF DISKETTE DRIVES
STOP PRINTERS
DISABLE AUDIO OUTPUT
86
READ SYSTEM PROFILE AREA
87
88
RE-SUME MODE SET ?
NO
YES
89
FORCE RESUME ?
YES
NO
90
HALT
91
ACTIVATE SUSPEND SAVE AREA
SAVE REAL TIME CLOCK INTERRUPT MODE
DISABLE ALL RTC INTERRUPTS EXCEPT ALARM INTERRUPT
92
93
POWER ON BY ALARM REQUESTED ?
YES
NO
94
ENABLE POWER-ON BY ALARM HDWR
95
A

FIG. 3A

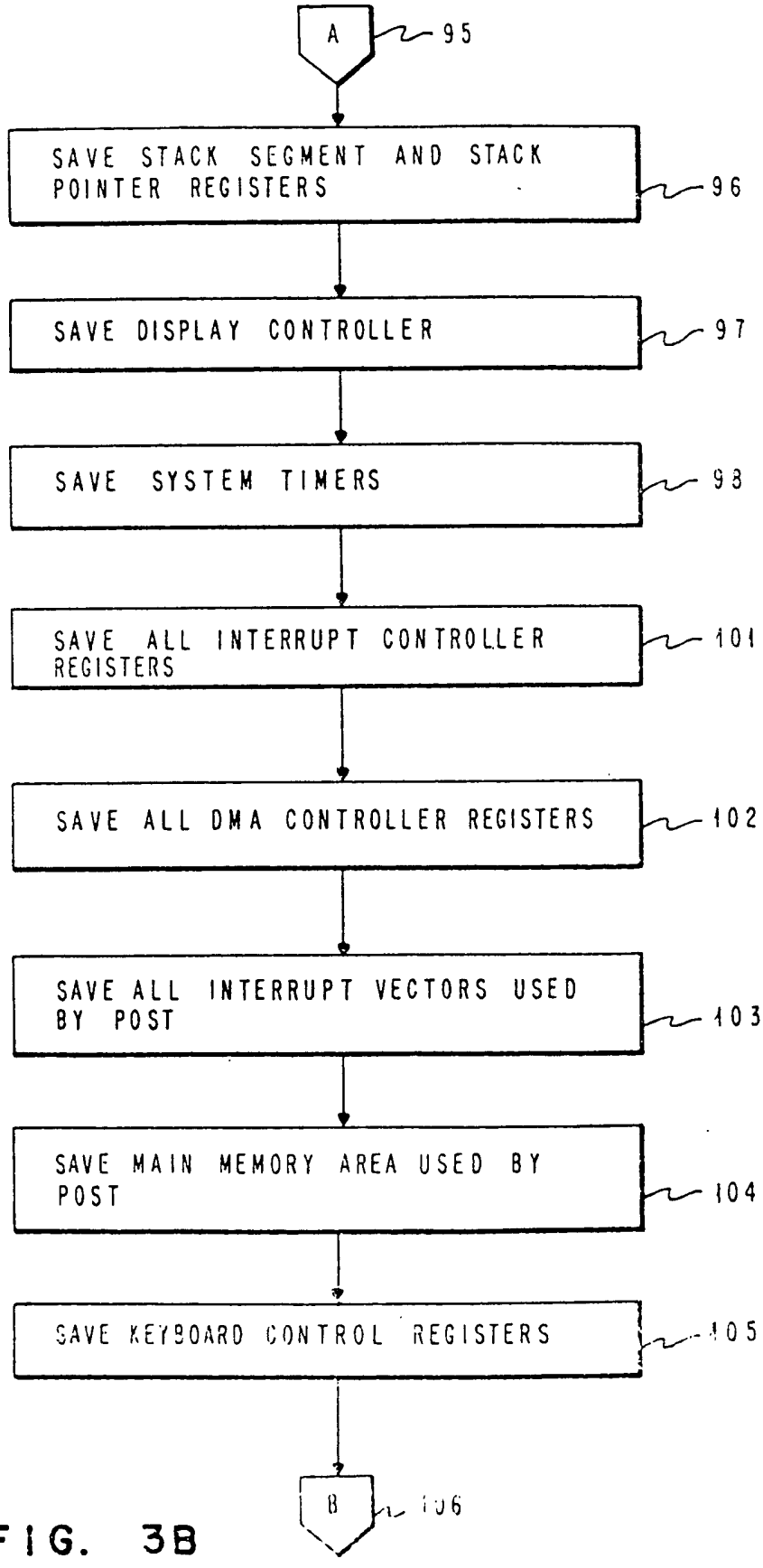
A
95
SAVE STACK SEGMENT AND STACK POINTER REGISTERS
96
SAVE DISPLAY CONTROLLER
97
SAVE SYSTEM TIMERS
98
SAVE ALL INTERRUPT CONTROLLER REGISTERS
101
SAVE ALL DMA CONTROLLER REGISTERS
102
SAVE ALL INTERRUPT VECTORS USED BY POST
103
SAVE MAIN MEMORY AREA USED BY POST
104
SAVE KEYBOARD CONTROL REGISTERS
105
B
106

FIG. 3B

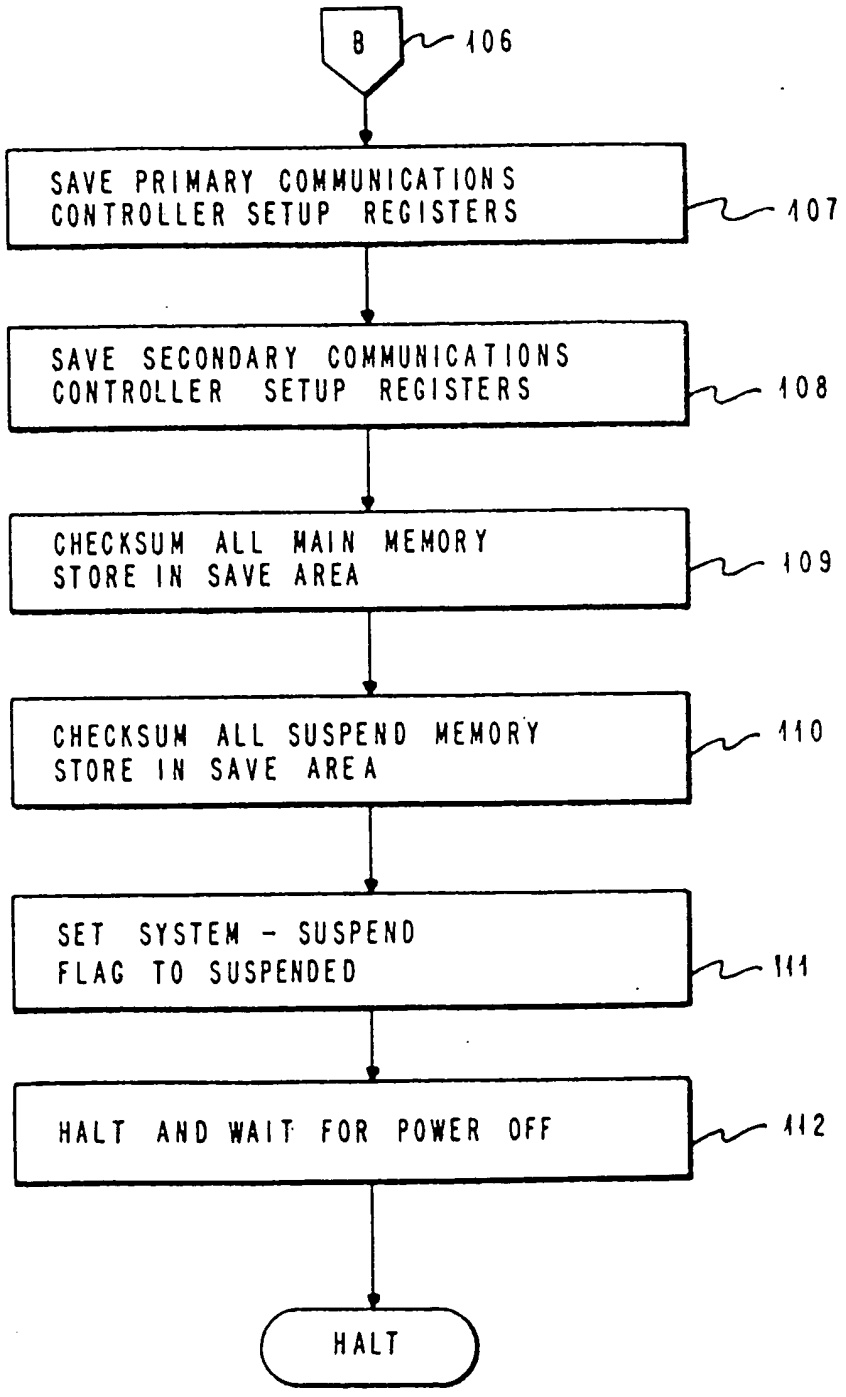
B
106
SAVE PRIMARY COMMUNICATIONS CONTROLLER SETUP REGISTERS
107
SAVE SECONDARY COMMUNICATIONS CONTROLLER SETUP REGISTERS
108
CHECKSUM ALL MAIN MEMORY STORE IN SAVE AREA
109
CHECKSUM ALL SUSPEND MEMORY STORE IN SAVE AREA
110
SET SYSTEM - SUSPEND FLAG TO SUSPENDED
111
HALT AND WAIT FOR POWER OFF
112
HALT

FIG. 3C

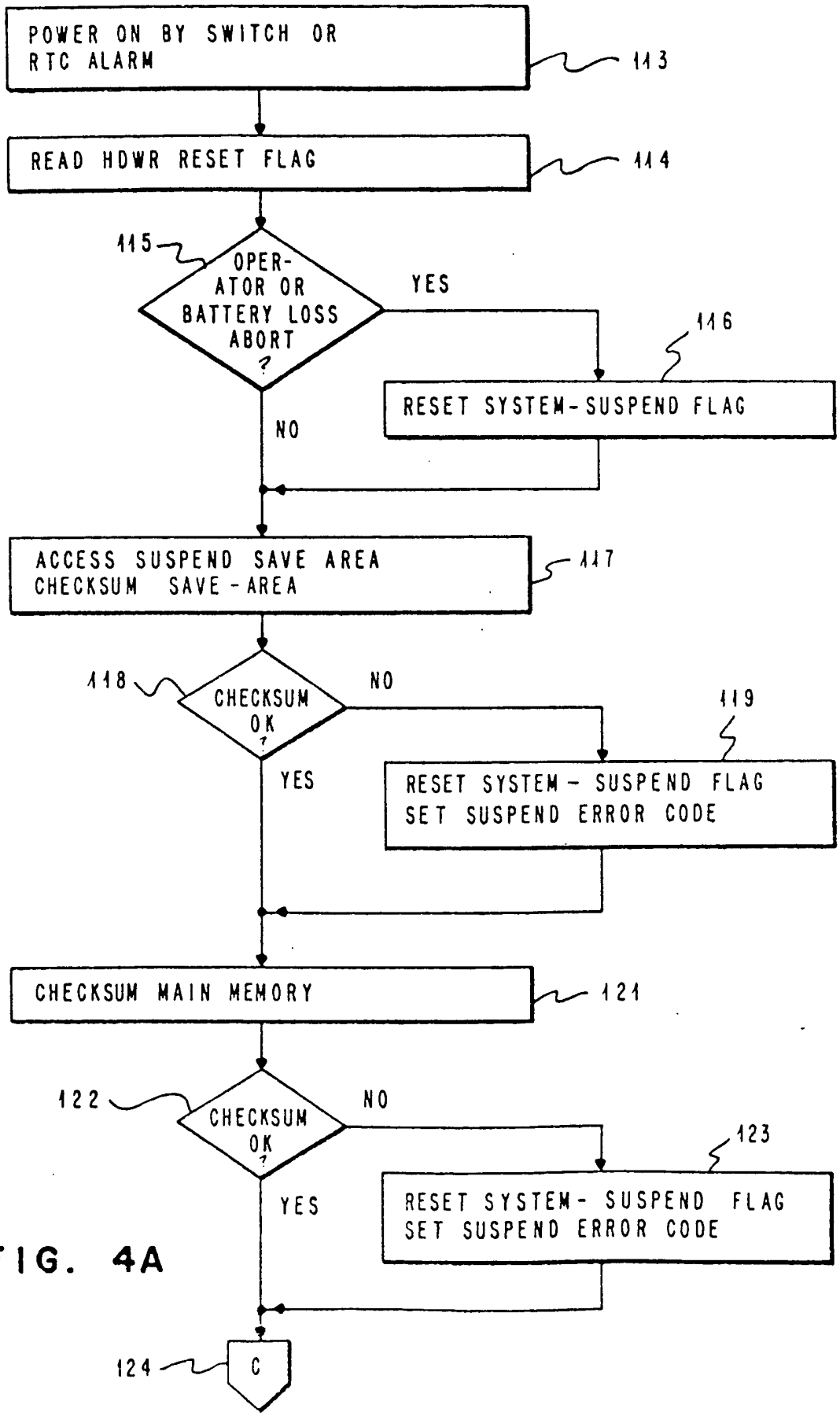
POWER ON BY SWITCH OR RTC ALARM
113
READ HDWR RESET FLAG
114
115
OPER-ATOR OR BATTERY LOSS ABORT ?
YES
116
RESET SYSTEM-SUSPEND FLAG
NO
ACCESS SUSPEND SAVE AREA CHECKSUM SAVE-AREA
117
118
CHECKSUM OK ?
NO
119
RESET SYSTEM - SUSPEND FLAG SET SUSPEND ERROR CODE
YES
CHECKSUM MAIN MEMORY
121
122
CHECKSUM OK ?
NO
123
RESET SYSTEM - SUSPEND FLAG SET SUSPEND ERROR CODE
YES
124
C

FIG. 4A

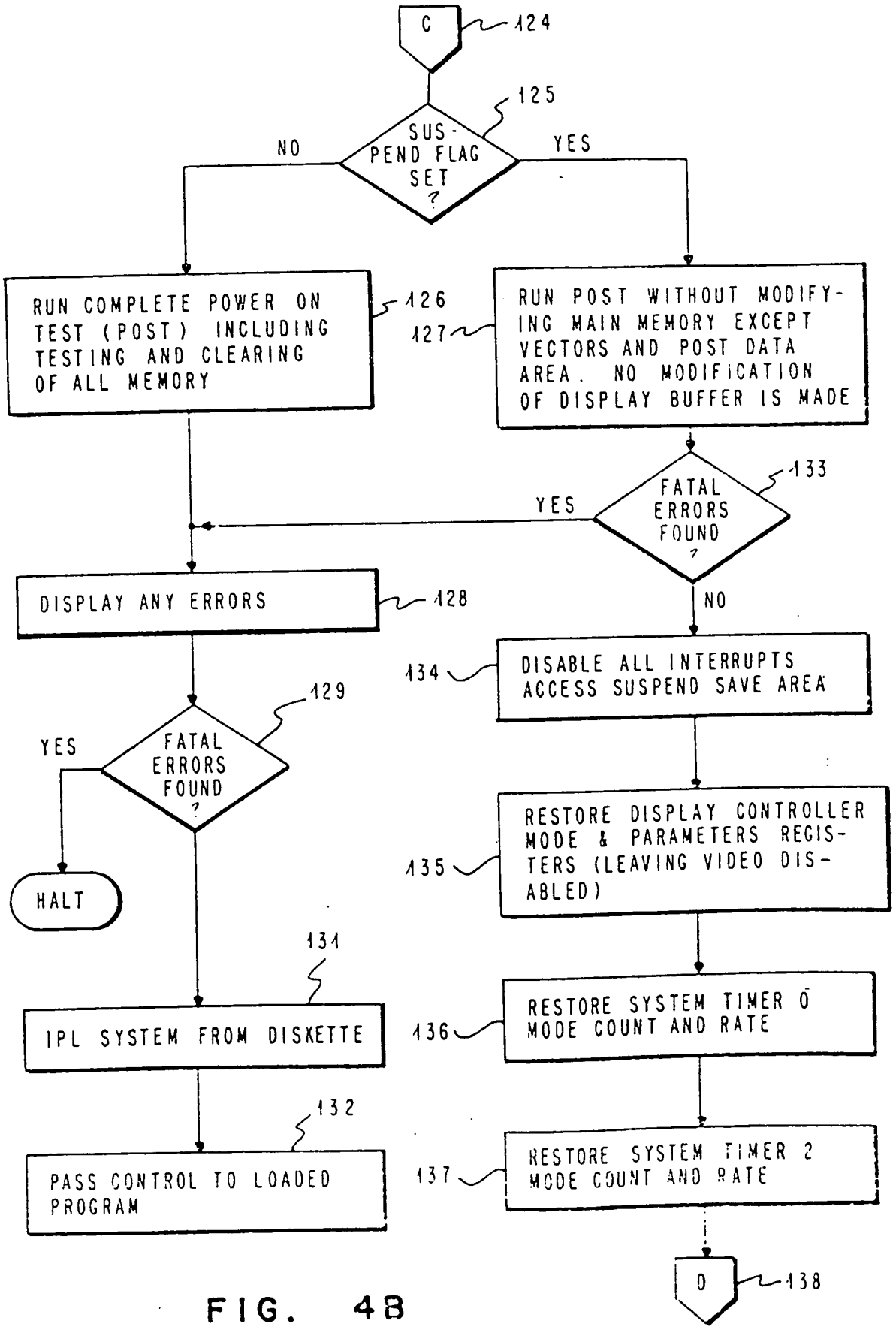
C
124
125
SUS-PEND FLAG SET ?
NO
YES
RUN COMPLETE POWER ON TEST (POST) INCLUDING TESTING AND CLEARING OF ALL MEMORY
126
127
RUN POST WITHOUT MODIFYING MAIN MEMORY EXCEPT VECTORS AND POST DATA AREA. NO MODIFICATION OF DISPLAY BUFFER IS MADE
FATAL ERRORS FOUND ?
133
YES
NO
DISPLAY ANY ERRORS
128
134
DISABLE ALL INTERRUPTS ACCESS SUSPEND SAVE AREA
129
FATAL ERRORS FOUND ?
YES
HALT
135
RESTORE DISPLAY CONTROLLER MODE & PARAMETERS REGISTERS (LEAVING VIDEO DISABLED)
131
IPL SYSTEM FROM DISKETTE
136
RESTORE SYSTEM TIMER 0 MODE COUNT AND RATE
132
PASS CONTROL TO LOADED PROGRAM
137
RESTORE SYSTEM TIMER 2 MODE COUNT AND RATE
D
138

FIG. 4B

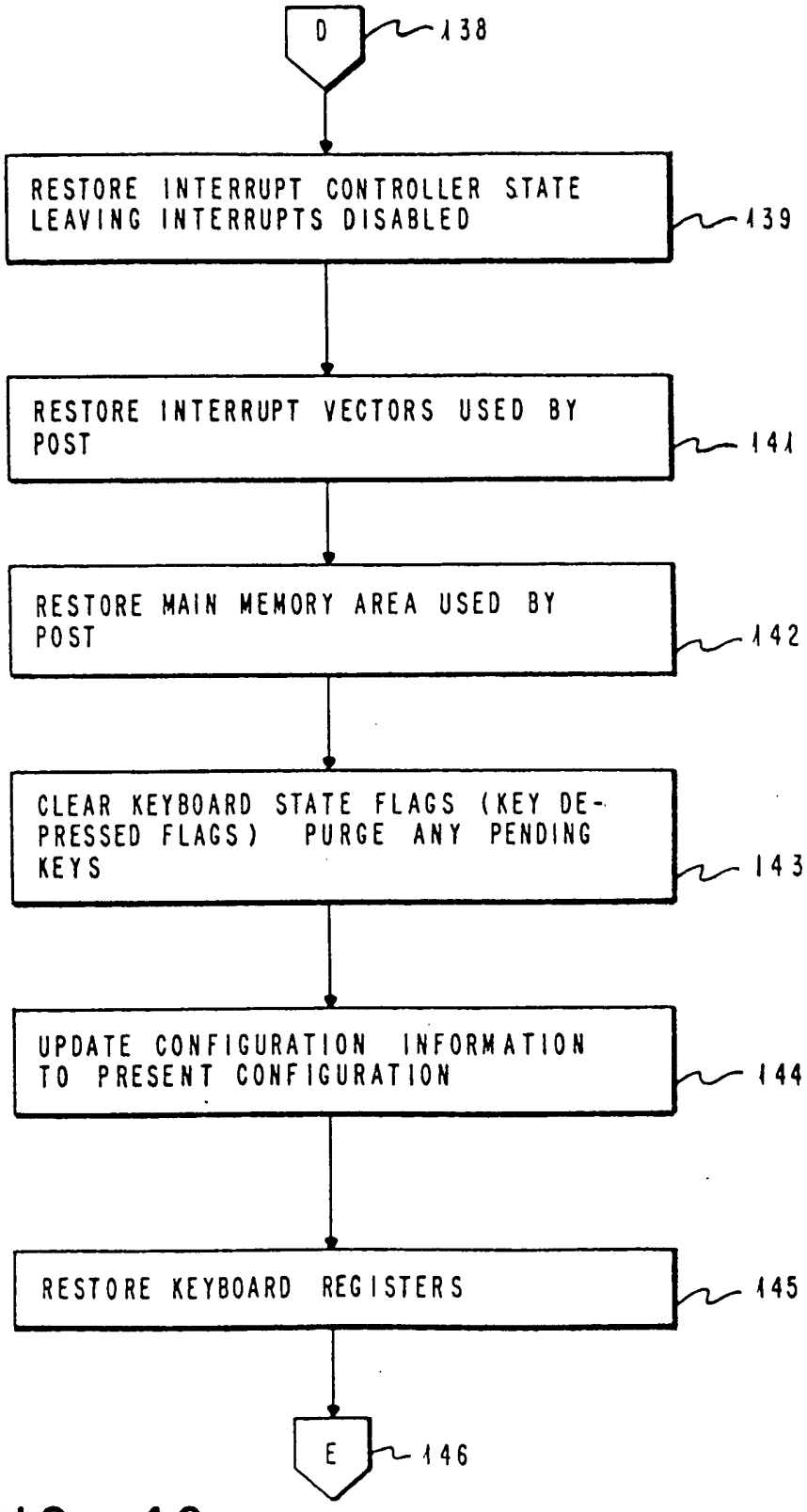
D
138
RESTORE INTERRUPT CONTROLLER STATE LEAVING INTERRUPTS DISABLED
139
RESTORE INTERRUPT VECTORS USED BY POST
141
RESTORE MAIN MEMORY AREA USED BY POST
142
CLEAR KEYBOARD STATE FLAGS (KEY DE-PRESSED FLAGS) PURGE ANY PENDING KEYS
143
UPDATE CONFIGURATION INFORMATION TO PRESENT CONFIGURATION
144
RESTORE KEYBOARD REGISTERS
145
E
146

FIG. 4C

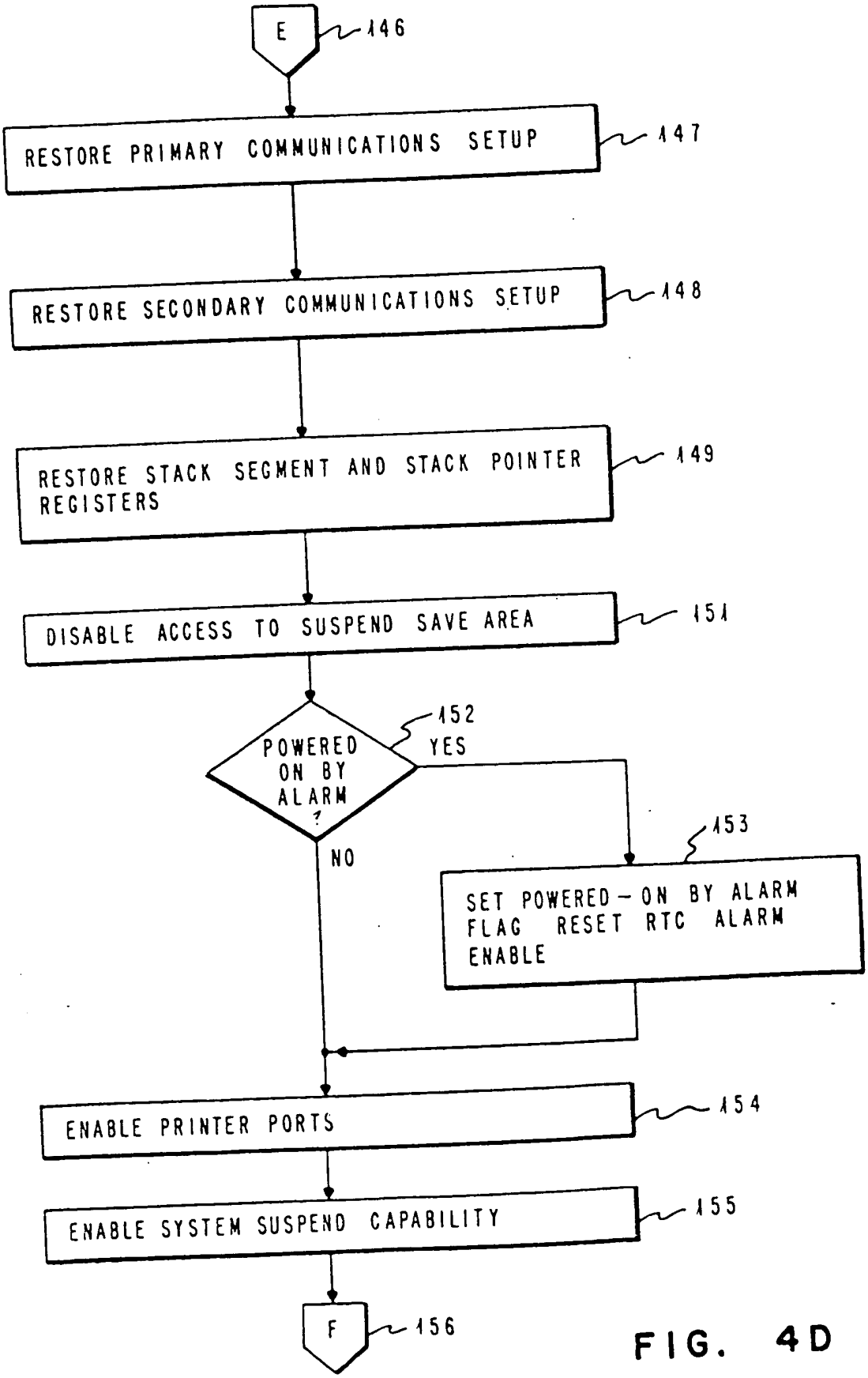
E
146
RESTORE PRIMARY COMMUNICATIONS SETUP
147
RESTORE SECONDARY COMMUNICATIONS SETUP
148
RESTORE STACK SEGMENT AND STACK POINTER REGISTERS
149
DISABLE ACCESS TO SUSPEND SAVE AREA
151
POWERED ON BY ALARM ?
152
YES
NO
153
SET POWERED-ON BY ALARM FLAG RESET RTC ALARM ENABLE
ENABLE PRINTER PORTS
154
ENABLE SYSTEM SUSPEND CAPABILITY
155
F
156

FIG. 4D

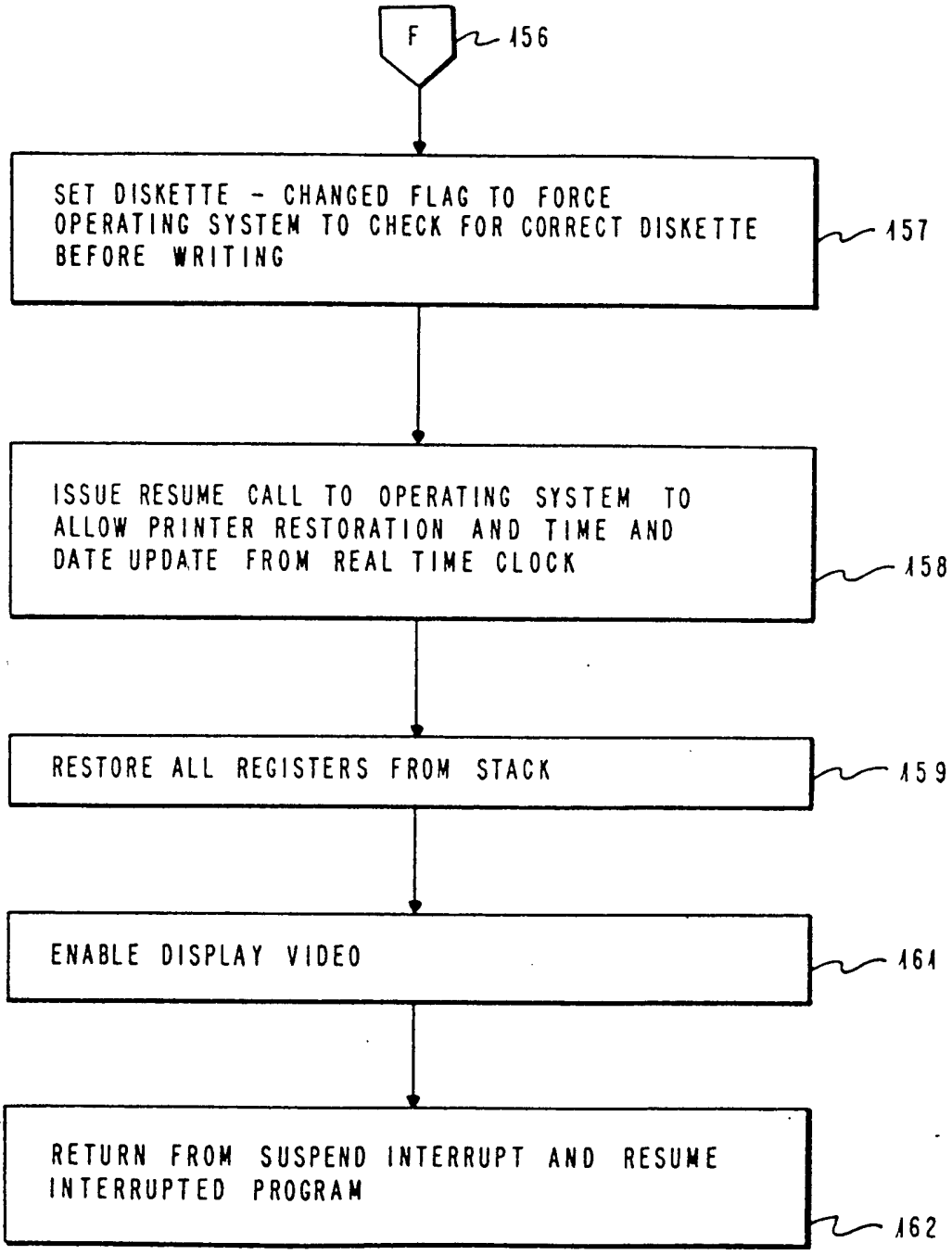
F
156
SET DISKETTE - CHANGED FLAG TO FORCE OPERATING SYSTEM TO CHECK FOR CORRECT DISKETTE BEFORE WRITING
157
ISSUE RESUME CALL TO OPERATING SYSTEM TO ALLOW PRINTER RESTORATION AND TIME AND DATE UPDATE FROM REAL TIME CLOCK
158
RESTORE ALL REGISTERS FROM STACK
159
ENABLE DISPLAY VIDEO
161
RETURN FROM SUSPEND INTERRUPT AND RESUME INTERRUPTED PROGRAM
162

FIG. 4E